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10/052,277	01/17/2002	Jensen Hartrung Jensen	US028005	4820

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EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 09/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,277	JENSEN, JENSEN HARTRUNG	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-13 and 15-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-13 and 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt was acknowledged of the Substitute Response filed on 21st of February 2006. Claims 11 and 13 had been amended; no claim had been canceled; and no claim had been newly added since the Final Office Action was mailed on 3rd of August 2005.

2. Receipt is acknowledged of the Amendment filed on 14th of August 2006. Claims 1, 10, and 15 have been amended; no claim has been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 13th of February 2006. Currently, claims 1-8, 10-13, and 15-19 are pending in this Application.

Specification

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the specification fails to provide the claimed limitation "the bus controller includes one or more devices that operate in dependence up the enabling signal" in lines 1-2 of the claim 8 under a proper antecedent basis.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. However, the limitation "the bus controller includes one or more devices that operate in dependence up to the enabling signal" in lines 1-2 of the claim 8 is not shown in the drawings. Therefore, the limitation must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended.

The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-8, 10-13 and 15-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Mitchell et al. [US 5,987,614 A; hereinafter Mitchell].

Referring to claim 1, Mitchell discloses a system (i.e., distributed power management system; See col. 1, lines 5-10) comprising:

- a plurality of components (i.e., Subsystem 1, ... Subsystem n in Fig. 3) each having a bus interface (i.e., Clock Gate Logic 53 and Bus I/F 54 in Fig. 3),
- a bus structure (i.e., Data 71, Address 72, Bus Controls & Status 73, and Bus Clock 74 in Fig. 3) that is configured to facilitate communications among said plurality of components (See col. 7, lines 39-44), and

- an activity detector (i.e., Central PMU 42 of Fig. 3; See col. 6, lines 47-50) that is configured to detect an initiation (i.e., detecting an occurrence of particular system resource activity; See col. 1, lines 32-44) of a data-transfer operation (i.e., bus cycle for data transfer; See col. 7, lines 39-54) and to provide therefrom an enabling signal (i.e., ON/DOZE/SLEEP/SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3; See col. 1, line 51 through col. 2, line 6) that is communicated to bus interfaces (i.e., said Clock Gate Logic and Bus I/F; See Fig. 3) of a plurality of said components (i.e., said Subsystem 1, ... Subsystem n; See col. 6, lines 50-58), wherein
    - said bus interface (i.e., said Clock Gate Logic and Bus I/F) is configured to be enabled to receive data from said bus structure (i.e., said Data, Address, Bus Controls & Status, and Bus Clock) as part of said data-transfer operation (i.e., said bus cycle for data transfer) upon receipt of said enabling signal from said activity detector (See col. 7, line 55 through col. 8, line 3 and col. 9, lines 54-61).

Referring to claim 2, Mitchell teaches

- said activity detector (i.e., Central PMU 42 of Fig. 3) is configured to detect a completion of said data-transfer operation (See col. 2, lines 25-31; i.e., detecting a completion of the particular bus cycle using a predetermined idle time), and terminates said enabling signal (i.e., ON→DOZE→SLEEP→SUSPEND) based on said completion of said data-transfer operation (i.e., based on said predetermined idle time; See col. 2, lines 31-44), and
- said bus interface (i.e., Clock Gate Logic 53 and Bus I/F 54 in Fig. 3) is configured to be disabled from receiving data from said bus structure upon termination of said enabling

signal (See col. 1, line 51 through col. 2, line 6; in fact, SUSPEND signal disables receiving data from bus structure).

Referring to claim 3, Mitchell teaches

- said enabling signal (i.e., ON/DOZE/SLEEP/SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3) includes a gated clock signal (i.e., said power down/up signal on said Power Down is directly input to Clock Gate Logic 53 in Fig. 3;See col. 9, lines 54-65).

Referring to claim 4, Mitchell teaches

- said bus interface (i.e., Clock Gate Logic 53 and Bus I/F 54 in Fig. 3) includes a plurality of clocked devices (i.e., Clock Gate Logic 63, Master I/F Block 86, and Slave I/F Block 88 in Fig. 5) that are clocked based on said enabling signal (i.e., said Clock Gate Logic, said Master I/F Block, and said Slave I/F Block are being clocked based on enabling status of ON/DOZE/SLEEP/ SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3).

Referring to claim 5, Mitchell teaches said activity detector (i.e., Central PMU 42 of in Fig. 3) includes:

- a set-reset device (i.e., Activity Monitors 21 of Fig. 1) that is set (i.e., operating to trigger a particular predetermined action) upon detection of said initiation of said data-transfer operation (i.e., upon the occurrence of one or more pre-identified addresses or address ranges on address bus; See col. 1, lines 44-50), and

- a delay device (i.e., Activity Timers 23 of Fig. 1), operably coupled to said set-reset device (i.e., said Activity Monitors and Activity Timers are operable coupled; See col. 2, lines 42-44), that is configured to provide said enabling signal (i.e., ON/DOZE/SLEEP/SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3) synchronous with a system clock (i.e., said Central PMU is synchronized with Bus Clock bclk 74 in Fig. 3) that is common to said bus structure (i.e., Data 71, Address 72, Bus Controls & Status 73, and Bus Clock 74 in Fig. 3; See col. 7, lines 38-43), based on whether said set-reset device is set (See col. 1, lines 31-50).

Referring to claim 6, Mitchell teaches

- said set-reset device (i.e., Activity Monitors 21 of Fig. 1) is reset (i.e., no triggering operation based on no activity being monitored on Address Bus 26 and Bus Controls 27 in Fig. 1) upon detection of a completion of said data-transfer operation (i.e., detecting of bus idle; See col. 2, lines 25-40).

Referring to claim 7, Mitchell teaches

- a bus controller (i.e., Central Bus Interface 43, in fact, Bus Arbiter Logic 130 in Fig. 3) that is configured to establish a communications path (i.e., communication path between Master device and Slave device; See col. 14, lines 58-65 and Fig 11) between an initiating component (i.e., any Subsystem requesting resources as said Master device on a target Subsystem in Fig. 3) of said plurality of components (i.e., Subsystem 1, ... Subsystem n in Fig. 3) and a target component (e.g., Subsystem 1 51 as said Slave device in Fig. 3) of said plurality of components,

- wherein said activity detector (i.e., Central PMU 42 of Fig. 3) provides said enabling signal (i.e., ON/DOZE/SLEEP/SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3; See col. 1, line 51 through col. 2, line 6) within a time duration consumed by said bus controller to establish said communications path (i.e., the time duration for establishing communication path from said Master device to said Slave device by way of arbitration is longer than the time duration for providing the enabling signal by way of monitoring bus activity because the communication path should be established for the communication between said Master device and said Slave device after the activity detector generates the enabling signal, which clearly anticipates said activity detector providing said enabling signal within a time duration consumed by said bus controller to establish said communications path; See col. 15, lines 5-15).

Referring to claim 8, Mitchell teaches said bus controller (i.e., Central Bus Interface 43 of Fig. 3) including

- one or more devices (i.e., Clock Div. Notify 44, Clock Freq. Control 45, Latency Timer 46, and Bus Arbiter Logic 130 in Fig. 3) that operate in dependence upon said enabling signal (i.e., said Central Bus Interface is operating in dependence upon Bus Clock(f2) from Central PMU 42 via host bus 41 in Fig. 3; See col. 3, lines 3-13).

Referring to claim 10, Mitchell discloses a method of reducing power consumption in a system (i.e., distributed power management system; See col. 3, lines 66-67) comprising

- a plurality of components (i.e., Subsystem 1, ... Subsystem n in Fig. 3) each having a bus interface (i.e., Clock Gate Logic 53 and Bus I/F 54 in Fig. 3), that are configured to communicate via a bus structure (i.e., Data 71, Address 72, Bus Controls & Status 73, and Bus Clock 74 in Fig. 3; See col. 7, lines 39-44), comprising:
    - detecting an initiation (i.e., detecting an occurrence of particular system resource activity) of a data-transfer operation (i.e., bus cycle for data transfer; See col. 7, lines 39-54) by a component of said plurality of components (See col. 1, lines 32-44),
    - communicating an enabling signal (i.e., ON/DOZE/SLEEP/SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3; See col. 1, line 51 through col. 2, line 6) to more than one other components of said plurality of components (i.e., said Subsystem 1, ... Subsystem n; See col. 6, lines 50-58), and
    - enabling a bus interface (i.e., Clock Gate Logic 53 and Bus I/F 54 in Fig. 3) at each of said more than one other components (i.e., said Subsystem 1 and Subsystem n) to receive data signals as part of said data-transfer operation (i.e., said bus cycle for data transfer), based on said enabling signal (i.e., said Clock Gate Logic, said Master I/F Block, and said Slave I/F Block are being clocked based on enabling status of ON/DOZE/SLEEP/ SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3).

Referring to claim 11, Mitchell teaches

- detecting a completion of said bus activity (See col. 2, lines 25-31; i.e., detecting a completion of the particular bus cycle using a predetermined idle time), and

- disabling said bus interface (i.e., Clock Gate Logic 53 and Bus I/F 54 in Fig. 3) at each of said more than one other components (i.e., Subsystem 1, ... Subsystem n in Fig. 3), based on said completion of said bus activity (See col. 1, line 51 through col. 2, line 6; in fact, SUSPEND signal disables receiving data from bus structure).

Referring to claim 12, Mitchell teaches

- synchronizing said enabling signal (i.e., ON/DOZE/SLEEP/SUSPEND signal and power down/up signal on Power Down 75 of Fig. 3) to a system clock (i.e., Central PMU 42 is synchronized with Bus Clock bclk 74 in Fig. 3) that is common to said bus structure (i.e., Data 71, Address 72, Bus Controls & Status 73, and Bus Clock 74 in Fig. 3; See col. 7, lines 38-43), based on whether said set-reset device is set (See col. 1, lines 31-50).

Referring to claim 13, Mitchell teaches

- establishing a communications path (i.e., communication path between Master device and Slave device; See col. 14, lines 58-65 and Fig 11) between said component that initiated said bus activity (i.e., any Subsystem requesting resources as said Master device on a target Subsystem in Fig. 3) and a target component (e.g., Subsystem 1 51 as said Slave device in Fig. 3) of said more than one other components (i.e., Subsystem 1 ... Subsystem n in Fig. 3), and
- enabling said bus interface (i.e., Clock Gate Logic 53 and Bus I/F 54 in Fig. 3) at said target component within a time duration required to establish said communications path (i.e., the time duration for establishing communication path from said Master device to said Slave device by way of arbitration is longer than the time duration for providing the enabling signal by way of monitoring bus activity because the communication path

should be established for the communication between said Master device and said Slave device after the activity detector generates the enabling signal, which clearly anticipates said activity detector providing said enabling signal within a time duration consumed by said bus controller to establish said communications path; See col. 15, lines 5-15).

Referring to claim 15, Mitchell discloses an electronic circuit (i.e., distributed power management system; See col. 1, lines 5-10) comprising:

- a plurality of initiators (i.e., Subsystem 1, ... Subsystem n in Fig. 3) that are configured to selectively initiate data-transfer operations (i.e., requesting resources which are included in target; See col. 7, lines 47-54) via a bus structure (i.e., Data 71, Address 72, Bus controls & status 73, Bus clock 74, Power down 75 and Central bus interface 43 in Fig. 3),
- an activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) that is configured to detect an initiation of a data-transfer operation from any of said plurality of initiators (See col. 7, lines 43-46 and 55-57; i.e., detecting a particular bus cycle), and to generate therefrom an enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3),
- a plurality of targets (i.e., Subsystem 1, ... Subsystem n in Fig. 3) that are configured to process said data-transfer operations (i.e., providing requested resources; See col. 7, lines 55-61), each of said plurality of targets (e.g., Subsystem 1 51 in Fig. 3) including
    - an interface (i.e., core logic 52, e.g., core logic 1 52a, in Fig. 3) for receiving said data-transfer operations, wherein

- said interface (i.e., said core logic) of each of said plurality of targets is configured to receive data of said data-transfer operations in dependence upon said enabling signal from said activity detector (See col. 7, line 59 through col. 8, line 3).

Referring to claim 16, Mitchell teaches

- said plurality of initiators (i.e., Subsystem 1, ... Subsystem n in Fig. 3) are configured to effect said data-transfer operations at a system clock speed (i.e., bus clock bclk in Fig. 8; in fact, all the Subsystems are operating under the system bus clock bclk 74 in Fig. 3), and
- said interface (i.e., core logic 52, e.g., core logic 1 52a, in Fig. 3) of each of said plurality of targets is configured to operate at said system clock speed (i.e., bclk speed in Fig. 8) only when said activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) provides said enabling signal (i.e., gbclk 57 in Fig. 3; See col. 13, line 40 through col. 14, line 13).

Referring to claim 17, Mitchell teaches said enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3) includes

- a clocking signal that operates at said system clock speed (i.e., a gated clock signal gbclk 67 from control gate logic 63 in Fig. 7).

Referring to claim 18, Mitchell teaches said activity detector is configured

- to detect a completion of said data-transfer operations (See col. 8, lines 3-5; i.e., detecting a completion of the particular bus cycle), and

- to terminate said generation of said enabling signal (e.g., disabling gbclk 57a of Fig. 3) based on a completion of said data-transfer operations (See col. 8, lines 5-8).

Referring to claim 19, Mitchell teaches

- a bus controller (i.e., Address Decode Logic 91 and Address Comparison Logic 92 in Fig. 4) that is configured to establish a communications path (See col. 18, lines 3-25 and Fig 16) between an initiator of said plurality of initiators (i.e., any one of Subsystems requesting resources on a target Subsystem in Fig. 3) and a target (e.g., Subsystem 1 51 in Fig. 3) of said plurality of targets,
    - wherein said activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) is configured to generate said enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3) within a time duration required by said bus controller to establish said communications path (i.e., the time duration for establishing communication path from CPU to Subsystem 1 is longer than the time duration for providing the enabling signal because the communication path should be established after the activity detector generates the enabling signal, which clearly anticipates said activity detector is configured to generate said enabling signal within a time duration required by said bus controller to establish said communications path; See col. 7, line 38 through col. 8, line 3 and Fig. 3).

Response to Arguments

7. Applicant's arguments filed on 14th of August 2006 have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to "In particular, the claims have been amended to make clear that an activity detector is configured to detect an initiation of a data-transfer operation on a common bus and to provide therefrom an enabling signal that is communicated to bus interfaces of a plurality of components coupled to the common bus through respective bus interfaces." in the Response page 6, lines 9-12, the Examiner notices that the features upon which applicant relies (i.e., to detect an initiation of a data-transfer operation on a common bus) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In fact, the Applicant has never recited the language "common bus" in the claimed invention.

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "Furthermore, the claims have been amended to make clear that such enabling allows a bus interface of a component to receive data of a data transfer operation so detected. ..." in the Response page 6, lines 13-18, the Examiner respectfully disagrees.

In contrary to the Applicant's allegation, Mitchell teaches the scope of the above argued element, such that enabling allows a bus interface (i.e., Clock Gate Logic and Bus I/F) of a component (i.e., Subsystem) to receive data of a data transfer operation (i.e., bus cycle for data transfer) so detected (See Mitchell, col. 7, line 55 through col. 8, line 3 and col. 9, lines 54-61). See paragraph 6 of the instant Office Action, Claims 1-8, 10-13 and 15-19 rejection under 35 U.S.C. 102(b) as being anticipated by Mitchell.

Thus, the Applicant's argument on this point is not persuasive.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you

would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christopher E. Lee
Primary Patent Examiner
Art Unit 2112

5 CEL/